What is claimed is:

1. A method, comprising:

forming a trench in a substrate;

at least partially filling said trench with a metal material to form a source contact buried in the substrate;

epitaxially growing a source region over the source contact;

epitaxially growing a channel region located adjacent the source region;

providing a gate dielectric on top of the channel region; and

forming a gate electrode on the gate dielectric.

2. The method of claim 1, wherein the substrate comprises a silicon on insulator (SOI) substrate including an insulator layer between a base substrate layer and a semiconductor layer, wherein the source region is epitaxially grown from the semiconductor layer and the channel region is epitaxially grown from the semiconductor layer, and wherein forming the trench comprises forming the trench to extend through the semiconductor layer and into the insulator layer.

3. The method of claim 2, wherein forming the trench further comprises forming the trench to extend through the semiconductor layer and the insulator layer and into the base substrate layer.

4. The method of claim 3, further comprising forming a layer of dielectric material which surrounds the source contact and isolates the source contact from both the insulator layer and the base substrate layer.

5. The method of claim 1, further comprising forming a silicide region between the top of the buried source contact and a bottom of the source region.

6. The method of claim 1, further comprising forming a layer of dielectric material which surrounds the source contact and isolates the source contact from the substrate.

7. The method of claim 6, further comprising forming a capacitor in the substrate wherein the source contact forms a first electrode of a capacitor and the layer of dielectric material forms a dielectric of said capacitor.

8. The method of claim 1, wherein the substrate has a bottom surface and further comprising forming a conductive element extending into the substrate from the bottom surface.

9. The method of claim 1, further comprising forming a gate contact extending from above the gate electrode to make electrical contact with the gate electrode.

10. The method of claim 9, wherein forming the gate contact comprises forming the gate contact to laterally extend beyond the gate electrode.

11. A method, comprising:

forming a trench extending into a substrate including an insulating layer and a semiconductor layer, wherein said trench extends through the semiconductor layer and at least partially into the insulating layer;

partially filling the trench in the insulating layer with a metal material to form a source contact;

epitaxially growing semiconductor material from said semiconductor layer to cover a top of the source contact with a source region;

converting the semiconductor layer adjacent the source region to form a channel region; and

forming an insulated gate electrode over the channel region.

12. The method of claim 11, further comprising forming a silicide at the top of the source contact that is in contact with said source region.

13. The method of claim 11, wherein converting the semiconductor layer comprises:

reducing a thickness of the semiconductor layer; and

epitaxially growing the channel region from the reduced thickness semiconductor layer.

14. The method of claim 11, wherein a top of the source contact is below an upper surface of the insulating layer of the substrate.

15. The method of claim 11, further comprising forming a layer of dielectric material which insulates the source contact.

16. The method of claim 15, further comprising forming a capacitor in the substrate wherein the source contact forms a first electrode of the capacitor and the layer of dielectric material forms a dielectric of said capacitor.

17. The method of claim 1, wherein the substrate has a bottom surface and further comprising forming a conductive element extending into the substrate from the bottom surface.

18. A method, comprising:

forming a trench in a substrate including an insulating layer and an overlying semiconductor layer, the substrate including a trench extending into the insulating layer;

at least partially filling the trench in the insulating layer with a metal material to form a source contact;

forming a source region made of semiconductor material adjacent the overlying semiconductor layer and lying on top of and in electrical contact with the source contact;

forming a channel region from the overlying semiconductor layer adjacent the source region; and

forming an insulated gate electrode over the channel region.

19. The method of claim 18, further comprising forming a layer of insulating material for isolating the source contact.

20. The method of claim 18, further comprising forming a silicide region between the source region and the source contact.

21. The method of claim 18, wherein forming the source region comprises epitaxially growing a first semiconductor material and wherein forming the channel region comprises epitaxially growing a second semiconductor material different from the first semiconductor material.

22. The method of claim 18, further comprising forming a conductive element extending into the substrate from a bottom surface thereof, said conductive element comprising one of a thermal dissipator or an electrical contact.

23. The method of claim 22, further comprising forming a capacitor with the source contact as a first electrode of said capacitor and the conductive element is a second electrode of said capacitor.

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